Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 44-47 without prejudice and amend claims 48-55 and 58-60 as follows:

1-43 (previously canceled)

44-47. (canceled)

48. (currently amended): An array processor comprising:

processing elements grouped into a plurality of clusters, wherein each processing element is identified as a node in a torus network;

a first cluster having a first plurality of processing elements, the number of processing elements in the first cluster being less than the number of nodes in the torus network ;

a first cluster switch~~,~~ to which each processing element of the first plurality of processing elements is connected ~~to the cluster switch~~; and

a cluster control line connected to the first cluster switch for carrying a control signal, the control signal controlling the operation of the first cluster switch to selectively establish a connection path between two processing elements of the first plurality of processing elements, wherein the two processing elements are transpose nodes of the torus network and wherein each connection path established through the first cluster switch is communicatively equivalent to a

~~separate wire~~ connection path between two nearest neighbor processing elements disposed in ~~a~~ the torus network.

49. (currently amended): The array processor of claim 48 further comprising:

a second cluster having a second plurality of processing elements~~,~~; and

a second cluster switch connected to the first cluster switch, each processing element of the second cluster connected to the second cluster switch, the first and second cluster switches being further operable to establish a connection path between one processing element of the first plurality of processing elements with a processing element of the second plurality of processing elements.

50. (currently amended): The array processor of claim 48 wherein each processing element ~~has~~ is uniquely identified with an identifier which represents a matrix coordinate for a matrix element of a matrix, the matrix having a number of matrix elements greater than the number of processing elements in the first cluster.

51. (currently amended): The array processor of claim 50 wherein each processing element of the first plurality of processing elements ~~has~~ is uniquely identified with a matrix coordinate which is the transpose of another processing element in the first plurality of processing elements or a matrix coordinate having equal indices.

52. (currently amended): The array processor of claim ~~51~~ 48 wherein the first cluster switch further comprises a first plurality of multiplexers to establish an intra-cluster connection path between two processing elements in the first plurality of processing elements.

53. (currently amended): The array processor of claim 52 wherein the first and second cluster ~~switch~~ switches each further comprises a second plurality of multiplexers for establishing ~~a~~ an inter-cluster connection path between a processing element in the first plurality of processing elements and a processing element within an adjacent cluster.

54. (currently amended): An array processor comprising:

a plurality of clusters, each cluster having a plurality of processing elements, each processing element having an identifier which represents a matrix coordinate for a matrix element of a matrix wherein the identifier is used to indicate if a processing element is adjacent or not adjacent to another processing element, the matrix having a number of matrix elements greater than the number of processing elements of any cluster;

a plurality of cluster switches, each cluster switch connecting two adjacent clusters, each cluster switch connected to each processing element in its associated cluster, each cluster switch operable to establish a ~~one~~ first connection path between a processing ~~elements~~ element and its corresponding transpose processing element located in the same cluster or a second connection path between adjacent processing elements located in adjacent clusters; and

a plurality of control lines controlling the plurality of cluster switches to select a connection path to establish between processing elements.

55. (currently amended): The array processor of claim 54 wherein the plurality of control lines carry signals to establish connection paths between nearest neighbor processing elements, each established connection path has an input direction and an output direction, the input direction is relative to the matrix coordinate ~~of~~ uniquely identifying the processing element

receiving from the input direction, the output direction is relative to the matrix coordinate of the processing element transmitting to the output direction.

56. (previously presented): The array processor of claim 55 wherein the input direction is North, South, East, or West.

57. (previously presented): The array processor of claim 56 wherein the output direction is North, South, East, or West and different from the established input direction.

58. (currently amended): The array processor of claim 54 wherein each processing element of each cluster has a matrix coordinate uniquely identifying each processing element which is the transpose of another processing element in the same cluster or a matrix coordinate having equal indices.

59. (currently amended): The array processor of claim 58 wherein each processing element's nearest matrix element neighbor is located ~~within the same cluster or~~ in an adjacent cluster.

60. (currently amended): A method of arranging processing elements within a plurality of clusters to perform matrix operations in parallel, the method comprising:

identifying processing elements to represent a matrix coordinate for a matrix element of a torus matrix, the torus matrix having a number of matrix elements greater than the number of processing elements in any one cluster;

grouping processing elements into each cluster such that each cluster contains non-adjacent processing elements and their transpose processing elements and a cluster switch, wherein each cluster switch is connected to an adjacent cluster through its cluster switch;

selecting at least two of the processing elements; and

establishing a communication path between the at least two of the processing elements.

61. (previously presented): The method of claim 60 wherein the establishing step further comprises establishing a communication path between two processing elements disposed within the same cluster.

62. (previously presented): The method of claim 60 wherein the establishing step further comprises establishing a communication path between two processing elements disposed in adjacent clusters.